



# **Phase Control Thyristor**

DS5941-3 April 2013 (LN30251)

### **FEATURES**

- Double Side Cooling
- High Surge Capability

### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

#### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR4330M52* DCR4330M50 DCR4330M45	5200 5000 4500	$\begin{split} T_{vj} = -40^{\circ}\text{C to } 125^{\circ}\text{C}, \\ I_{DRM} = I_{RRM} = 300\text{mA}, \\ V_{DRM}, V_{RRM}  t_p = 10\text{ms}, \\ V_{DSM}  \&  V_{RSM} = \\ V_{DRM}  \&  V_{RRM} + 100V \\ respectively \end{split}$

Lower voltage grades available. \*5000V @ -40°C, 5200V @ 0°C

#### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR4330M52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### **KEY PARAMETERS**

$V_{DRM}$	5200V
$I_{T(AV)}$	4325A
I <sub>TSM</sub>	53400A
dV/dt*	2000V/µs
dl/dt	400A/μs
	-

### \* Higher dV/dt selections available

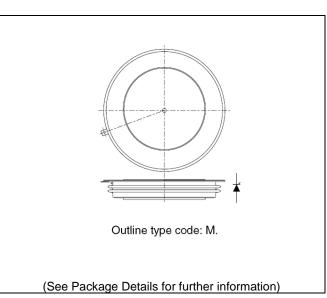


Fig. 1 Package outline





## **CURRENT RATINGS**

## $T_{\text{case}}$ = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Sid	de Cooled			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	4325	Α
I <sub>T(RMS)</sub>	RMS value	-	6790	А
I <sub>T</sub>	Continuous (direct) on-state current	-	6250	А

## **SURGE RATINGS**

Symbol Parameter		Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	53.4	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 0$	14.25	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.00518	°C/W
		Single side cooled	Anode DC	-	0.01012	°C/W
			Cathode DC	-	0.01080	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
T <sub>vj</sub>	Virtual junction temperature	Blocking V <sub>DRM</sub> / <sub>VRRM</sub>		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
Fm	Clamping force			74.0	91.0	kN





## **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125$ °C, ga	ite open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub>	Repetitive 50Hz	-	400	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	1000	A/µs
		$t_r < 0.5 \mu s, T_j = 125$ °C				
V <sub>T(TO)</sub>	Threshold voltage – Low level	1000 to 2600A at T <sub>case</sub> = 125	°C	-	0.85	V
	Threshold voltage – High level	2600 to 9000A at T <sub>case</sub> = 125	°C	-	0.99	V
r <sub>T</sub>	On-state slope resistance – Low level	1000 to 2600A at T <sub>case</sub> = 125°C		-	0.2115	mΩ
	On-state slope resistance – High level	2600 to 9000A at T <sub>case</sub> = 125°C		-	0.1578	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, $10\Omega$		-	3	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$T_j = 125$ °C, $V_R = 200$ V, dl/dt = 1A/ $\mu$ s,			750	μs
		dV <sub>DR</sub> /dt = 20V/μs linear				
Qs	Stored charge	1 - 2000 A T - 125°C - 41/44 - 4 A / 10		4030	5420	μC
I <sub>RR</sub>	Reverse recovery current	- $I_T = 3000A$ , $T_j = 125^{\circ}C$ , $dI/dt - 1A/\mu s$ , $V_{Rpeak} \sim 3100V$ , $V_R \sim 2100V$		49	59	A
IL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	А
IH	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500A, I_T = 5A$		-	300	mA





### **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	400	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

## **CURVES**

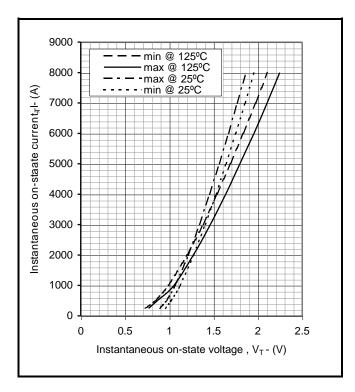


Fig.2 Maximum & minimum on-state characteristics

 $V_{TM}$  **EQUATION** Where A = 0.061592

B = 0.115333

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$  C = 0.000119 D = 0.002394

these values are valid for  $T_j = 125$ °C for  $I_T 250$ A to 9000A



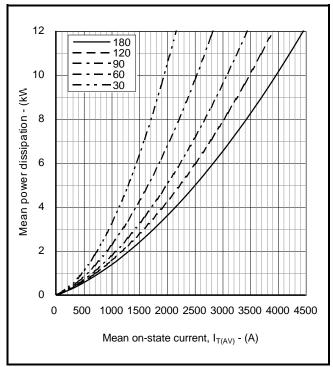


Fig.3 On-state power dissipation - sine wave

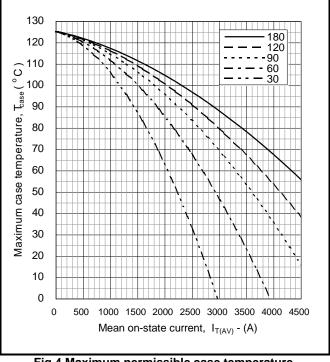


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

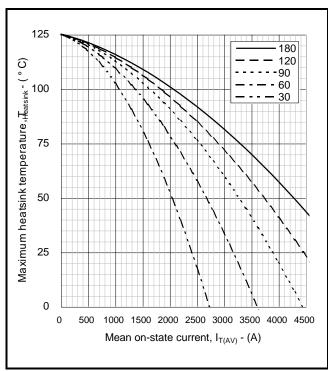


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

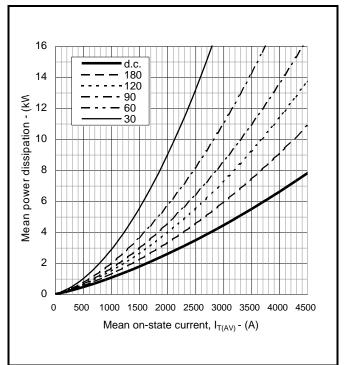


Fig.6 On-state power dissipation - rectangular wave



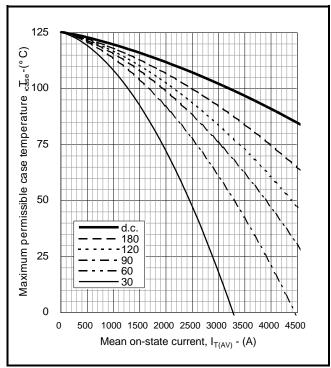


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

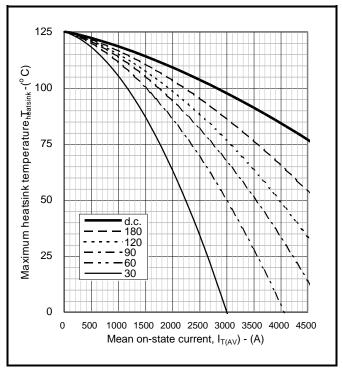
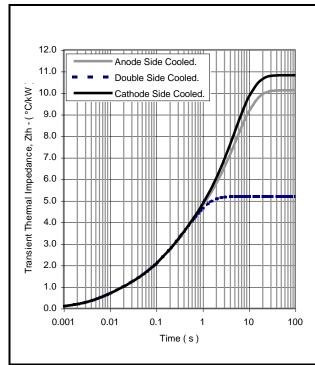


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	1.995338	1.242784	1.9448	0.005
Double side cooled	T <sub>i</sub> (s)	0.05	0.592935	0.592385	110.5108
Anode side cooled	R <sub>i</sub> (°C/kW)	6.092995	1.957372	2.042252	0.035908
	T <sub>i</sub> (s)	5.459764	0.510898	0.05	110.1735
Cathode side cooled	R <sub>i</sub> (°C/kW)	6.856845	1.876401	2.062845	0.025343
Callibue side cooled	T; (s)	5.181139	0.557321	0.05	110.1546

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

## $\Delta R_{th(j-c)}$ Conduction

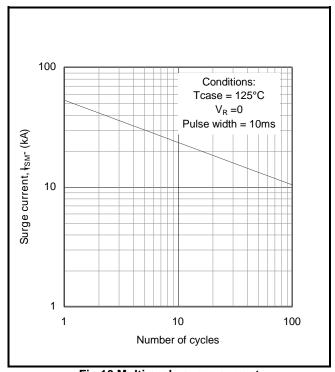
Tables show the increments of thermal resistance  $R_{\text{th(j-c)}}$  when the device operates at conduction angles other than d.c.

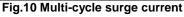
Double side cooling				Ar	node Side	C		
	$\Delta Z_{th}$ (z)				$\Delta Z_t$	<sub>h</sub> (:		
θ°	sine.	rect.		θ°	sine.			
180	0.51	0.36	ĺ	180	0.51			
120	0.57	0.49	ĺ	120	0.58			
90	0.64	0.56	i	90	0.65			
60	0.70	0.63	i	60	0.71			
30	0.74	0.71		30	0.75			
15	0.76	0.74		15	0.77			

	$\Delta Z_{th}$ (z)			
θ°	sine.	rect.		
180	0.51	0.36		
120	0.58	0.50		
90	0.65	0.57		
60	0.71	0.64		
30	0.75	0.71		
15	0.77	0.75		

Fig.9 Maximum (limit) transient thermal impedance - junction to case (°C/kW)







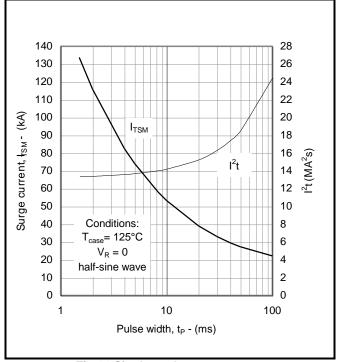


Fig.11 Single-cycle surge current

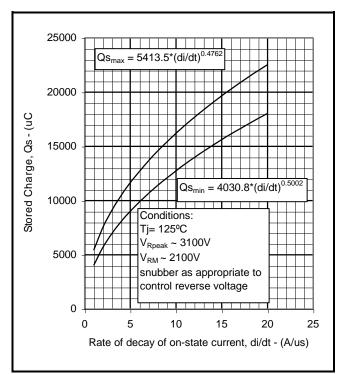


Fig.12 Stored charge

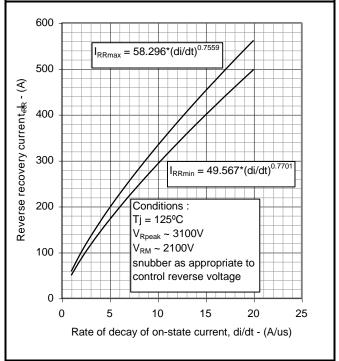


Fig.13 Reverse recovery current

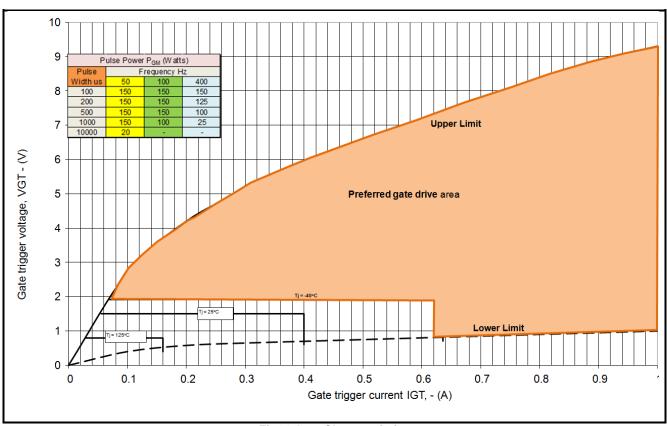


Fig14 Gate Characteristics

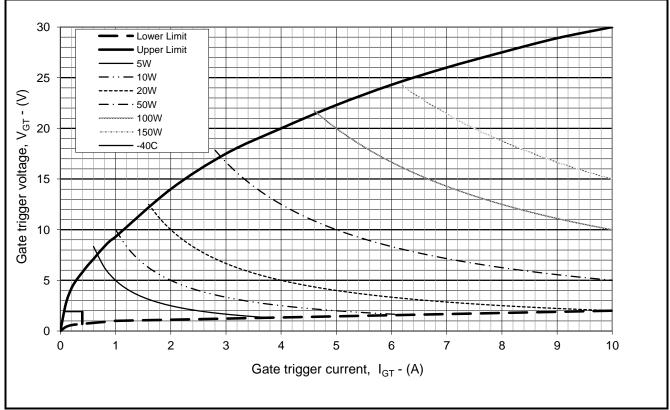


Fig. 15 Gate characteristics



### **PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

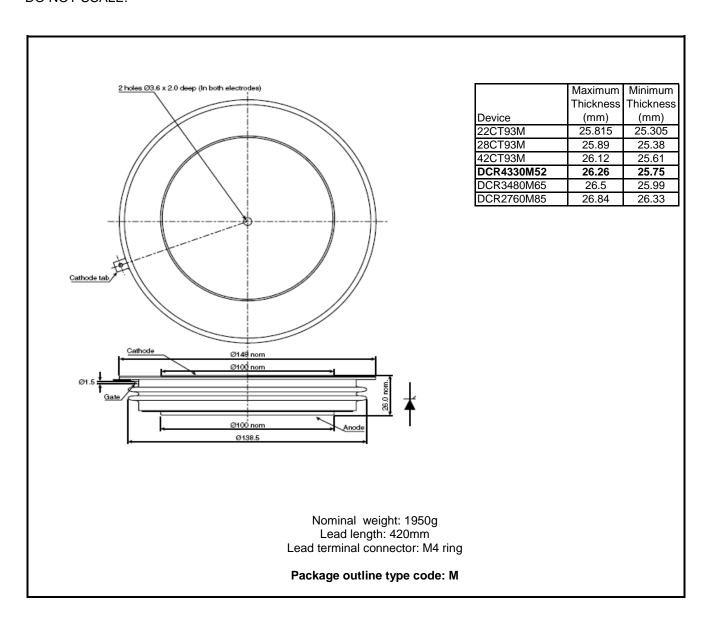


Fig.16 Package outline





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### **HEADQUARTERS OPERATIONS**

DYNEX SEMICONDUCTOR LIMITED

Doddington Road, Lincoln, Lincolnshire, LN6 3LF

United Kingdom.

Phone: +44 (0) 1522 500500 Fax: +44 (0) 1522 500550 Web: http://www.dynexsemi.com

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### **CUSTOMER SERVICE**

Phone: +44 (0) 1522 502753 / 502901 Fax: +44 (0) 1522 500020

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